Optimization of Channel Profiles for Ultra-Short MOSFETs by Quantum Simulation

1996

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Abstract

In this paper, the self-consistent solution of 1-D Poisson and Schrödinger equations is performed on doping profiles suitable for the fabrication of advanced ultra-short n-MOSFETs. Different issues are considered and investigated, including quantum-induced threshold voltage shifts, low-field electron effective mobility and gate-to-channel capacitance. The reported results give indications for the optimization of n-MOS channel doping profiles.

In addition, the more advanced double-gate structure is analyzed and the reasons for possible advantages over more conventional single-gate ones (either SOI- or bulk-type) are investigated.

Introduction

In order to limit 2D short-channel effects (SCE) in ultra-short (US-) MOSFETs with gate length (L_G) in the 0.1 μm range and below, high doping levels ($\approx 10^{18}$cm^{-3}) and thin gate oxide ($\approx$ 3 nm) are required [1]. Consequently, the transverse electric field (TEF) is increased causing electron energy quantization and degradation of low-field mobility ($\mu_{\rm eff}$) [2]. In addition, as t_{OX} is reduced, the gate-to-channel capacitance is degraded, due to charge displacement from the interface [3]. Therefore, theoretical studies based on semi-classical models, aiming at the optimization of the channel doping profile [4], must be extended to account for the effects of energy quantization. Previous studies have been devoted to the analysis of the quantum deviations of threshold voltages caused by high dopings [2], and to the effects of quantization on the inversion-layer capacitance [3] in devices featuring almost uniform channel profiles within the MOS depletion layer. In this study, self-consistent 1D Poisson-Schrödinger calculations [5] are performed using non-uniform doping profiles, which are more realistic for the fabrication of US-MOSFETs. As a case study, quantum effects in an epitaxial-channel (EPI) MOS structure are investigated. In order to compare different channel doping profiles, three different macroscopic quantities are evaluated: i) quantum-induced threshold voltage shift; ii) electron low-field mobility; iii) MOS capacitance, including the effect of charge displacement from the interface.

The results obtained in this study put in evidence that quantum phenomena in MOS inversion layers are not simply related to doping values close the Si-SiO_2 interface, but a more complex relationship holds, involving the actual doping profile within a range of a few tenths of a micron away from the interface. Furthermore, this study provides design guidelines for the optimization of channel doping profiles, to be traded-off with those related to 2D SCE limitations.

In this paper, the self-consistent Poisson-Schrödinger solution is performed also on double-gate MOSFETs (DGM), in order to investigate possible advantages of such devices over single gate bulk and SOI MOSFETs, due to the so-called *volume-inversion* [6, 7].

Results

Silicon MOSFETs with epitaxial channel: Fig.1 provides a simple sketch of an ideal doping profile that can be obtained by epitaxial growth. A low-doped EPI is grown over a highly doped region, acting as a ground plane to suppress punch-through.

Examples of simulations of inhomogeneous channels are given in Figs.2,3 referring to structures with N_A=1×10^{18} cm^{-3}, N_{EPI}=1×10^{15} cm^{-3}, t_{OX}=3nm, inversion charge sheet density N_S=3×10^{12} cm^{-2}, and different t_{EPI}. For increasing t_{EPI}, charge confinement is reduced and the TEF in the depletion region becomes lower.

The case t_{EPI}=10 nm, t_{OX}=3 nm, investigated in [4] for application to MOSFETs with L_G down to 50 nm, is evaluated and its threshold voltage V_{TH} (computed from the simulated inversion charge Q_S vs. voltage characteristic) is compared with that of the highly-doped uniform devices. Fig.4 shows the threshold voltage shift with respect to the classical solution (quantum-induced threshold voltage shift, Q-DV) for the two structures and different oxide thicknesses. Due to the low surface doping, a much lower Q-DV could be expected in the EPI case, compared to HDU. Instead, comparable Q-DV is obtained for EPI and HDU, showing that this effect does not simply depend on the doping at the interface. Rather, a long-range de-

pendence on doping holds. This result clearly shows that simple models based on average channel doping values cannot be applied to the highly non-uniform cases needed for US-MOSFETs. This point is clarified by Fig.5, where Q-DV is reported as a function of t_{EPI}: a relatively thick EPI is needed to eliminate quantum effects related to the high-doped ground plane. Fig.6, instead, shows how V_{TH} can be controlled by properly selecting t_{EPI}.

The problem of channel μ_{eff} can be addressed looking at Figs.2,3. The introduction of low-doped EPI effectively decreases the TEF, as reported in Fig.7 showing the effective electric field (EEF) as a function of t_{EPI}, for given inversion charge sheet density. EFF is computed starting from the self-consistent charge and TEF distributions:

$$E_{EFF} = \frac{\int_0^\infty E(x)n(x)dx}{\int_0^\infty n(x)dx}$$

where x, $n(x)$ and $E(x)$ are the distance from the device surface, the electron density, and the TEF, respectively.

The corresponding μ_{eff} , extracted from universal mobility curves [8], are also given in Fig.7. It should be mentioned that, due to Coulomb scattering by unscreened impurities, the HDU is expected to present even larger disadvantages for low inversion charge densities [8].

Another important issue relates to total MOS capacitance (C_{TOT}, series of $C_{OX}=\varepsilon_{OX}/t_{OX}$ and $C_{INV}=dQ_S/d\phi_S$, where ϕ_S is the Si-surface potential) which reduces with respect to C_{OX} as t_{OX} is decreased, due to inversion charge displacement from the interface. As shown in [3] for uniform channels, such a reduction becomes more severe for lower dopings. Therefore, a lower capacitance should be expected for the EPI case, compared to the HDU one. Fig.8 reports $C_{TOT}=dQ_S/dV_G$ as a function of t_{OX}, for t_{EPI}=10 nm and 0 nm, showing that the capacitance degradation increases at thinner oxides, but no additional degradation occurs by introducing a thin low-doped EPI. As reported in Fig.9, the results of simulations indicate that for application to US-MOSFETs (t_{EPI} up to 30-40 nm [4]) no serious degradation shall be expected.

Double gate and SOI MOSFETs: we simulated a 1-D DGM structure to investigate its possible advantages over single-gate devices (see Fig.10). In particular, an increase of device current and transconductance, exceeding the factor of two related to the existence of two channels, was reported in [6, 7], and a different charge distribution within silicon, namely the presence of *volume inversion*, was invoked as a possible origin of this effect. In fact, a large amount of carriers displaced from the interface could give rise to higher μ_{eff} due to reduced interface scattering. More recently, a much lower effect of *volume inversion* was found [9], leading to the debate in [10]

In Fig.11, the charge distribution of a DGM structure with t_{SI}=10 nm and t_{OX}=3 nm is reported and compared to that of a single gate SOI (S-SOI) with same silicon and oxide thicknesses, a 50 nm back-oxide and a p-polysilicon gate that plays the role of silicon bulk. When the two structures are biased at the same V_G-V_{TH}, the DGM charge distribution is more displaced from the interface than the profile obtained summing the charge profiles of two specular S-SOI (dashed line). Furthermore, electric field are different for the two structures because in the DGM the TEF vanishes at the middle of the silicon layer. As a consequence, the EEF is lower in the DGM case, as shown in Fig.12, reporting the EEF for the two structures as a function of t_{EPI}. In this comparison, the inversion charge for the DGM is set to be two times that of the S-SOI MOS to account for the double channel. The EEF for the DGM is always lower than the S-SOI one. As t_{SI} is increased, the EEF increases towards the bulk value that is reached for non fully-depleted S-SOI and DGM.

Conclusions

In this work a self-consistent Schrödinger-Poisson simulator has been applied to the study of highly non-uniform doping profiles suitable for the fabrication of US-MOSFETs. The obtained results prove that a non trivial dependence of quantum effects on doping profile holds. Guidelines for the optimization of channel doping profiles are given. Applications to double-gate and single-gate SOI MOS structures have been reported. The results indicate that an improvement of currents and transconductance of the DGM with respect to S-SOI can be related to a different distribution of carriers within the silicon film and to a lower effective electric field.

Acknowledgements: The authors are grateful to Prof. C Jacoboni for the many discussions. One of the authors (A.A.) thanks A.R.O., O.N.R, and E.R.O. for partially funding the work.

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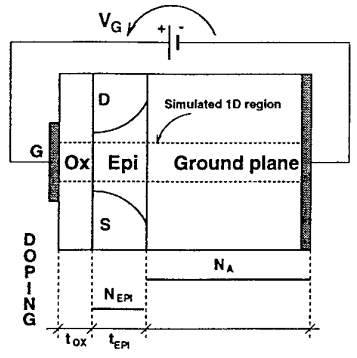

Figure 1: Schematic section and doping profile of the simulated structure.

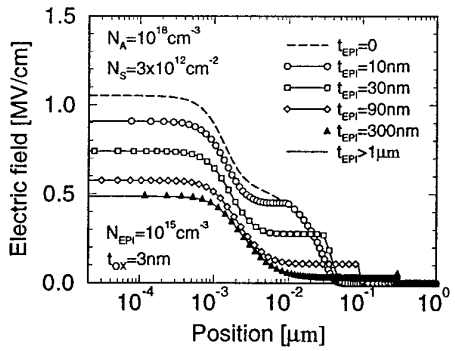

Figure 2: Transverse electric field for different EPI thicknesses. The x axis is in log scale to enlarge the inversion layer region. Symbols are for visualization only and do not correspond to actual discretization points.

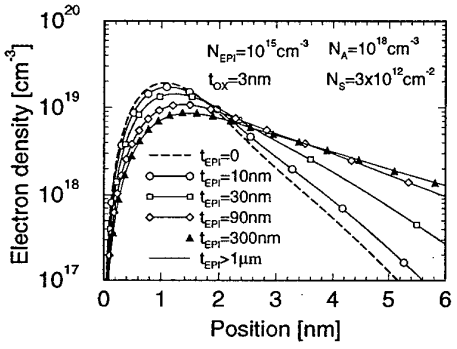

Figure 3: Electron density vs. position for different EPI thicknesses. Symbols are for visualization only and do not correspond to actual discretization points.

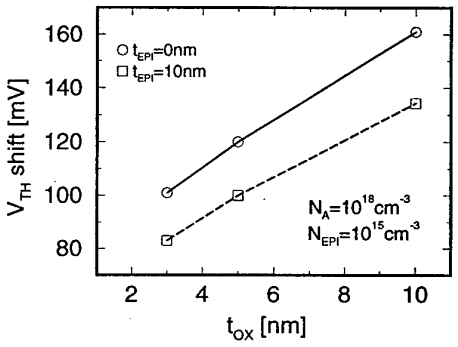

Figure 4: Quantum induced V_{TH} shift vs. oxide thickness.

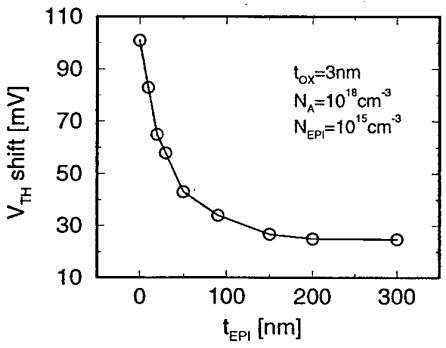

Figure 5: Quantum induced V_{TH} shift vs. EPI thickness.

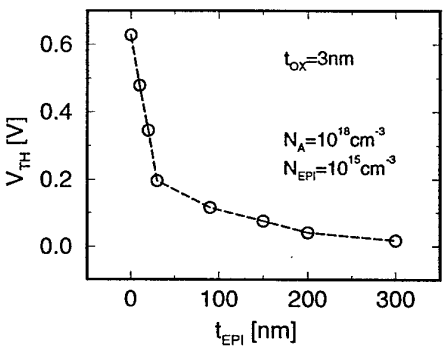

Figure 6: V_{TH} vs. EPI thickness.

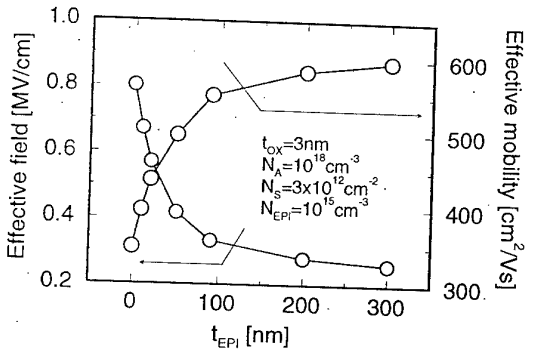

Figure 7: Effective electric field (squares, left) and effective mobility (circles, right) vs. EPI thickness. The bias V_G was set in order to obtain the same charge sheet density for all structures

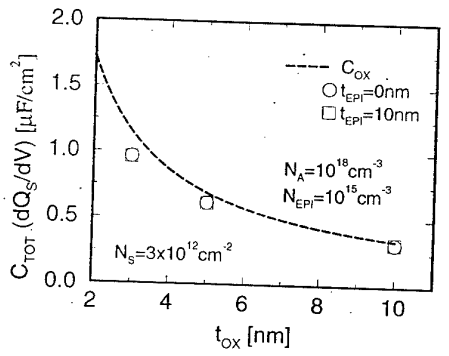

Figure 8: Total capacitance vs. oxide thickness. Symbols: simulated results. Dashed-line: C_{OX}. The bias V_G was set in order to obtain the same charge sheet density for all structures

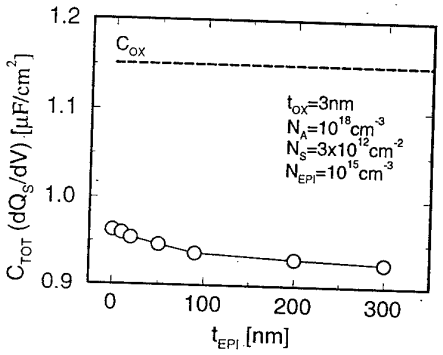

Figure 9: Total capacitance vs. t_{EPI}. Symbols: simulated results. Dashed-line: C_{OX}. The bias V_G was set in order to obtain the same charge sheet density for all structures

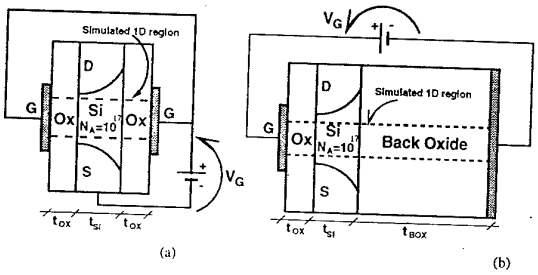

Figure 10: Schematic section of (a) the simulated DGM and (b) S-SOI structures. Doping concentration is uniform, $N_A=10^{17}$ cm^{-3}. In the S-SOI, a p-Poly gate accounts for the silicon bulk

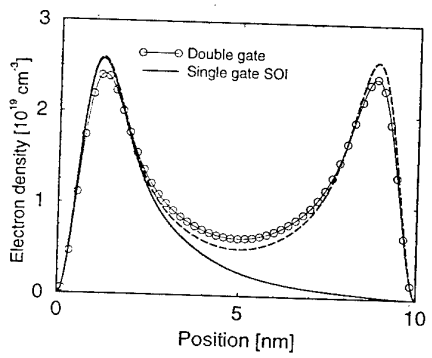

Figure 11: Electron density in the silicon film of a DGM structure (symbols) and a S-SOI one (solid line). V_G-$V_{TH}\simeq$1.0V, t_{SI}=10 nm, t_{OX}=3 nm for both structures. Dashed line: sum of two specular S-SOI charge profiles.

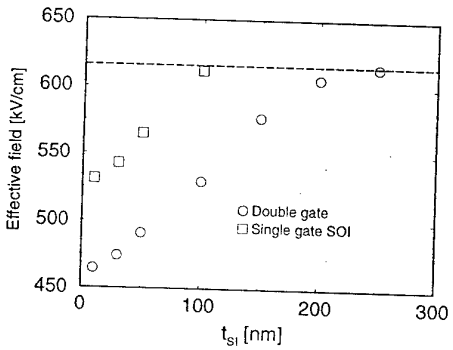

Figure 12: Effective electric field vs. silicon layer thickness for the DGM (N_{INV}=1.2 $\times$ 10^{13} cm^{-3}) and the S-SOI (N_{INV}=6 $\times$ 10^{12} cm^{-3}) structures. Dashed line: effective electric field for a uniform bulk MOS of same doping.